

Method and Apparatus for Improving Performance Margin in Logic Paths

ABSTRACT OF THE DISCLOSURE

An apparatus and method is disclosed for improving timing margins of logic paths on a semiconductor chip. Typical logic embodiments, such as CMOS (Complementary Metal Oxide Semiconductor), have path delays that become shorter as supply voltage is increased. Embodiments of the present invention store product data on each particular chip. The product data includes, for examples, but not limited to, a voltage range having a low limit voltage and a high limit voltage, a limit temperature, and performance of the particular chip in storage for the particular chip. Each chip has a voltage controller, a timer, and a thermal monitor. The voltage controller communicates with a voltage regulator and dynamically causes a voltage supply coupled to the chip to be as high as possible in the voltage range, subject to the limit temperature.